Analysis of Multiwalled Carbon Nanotube as On-Chip Interconnect

R. Gayathri*, T. Abirami

Department of Electronics and Communication, M. Kumarasamy College of Engineering, Karur-639 113

***Corresponding author: E-Mail: gaayathriece@gmail.com**

ABSTRACT

The historical understanding of the interconnect problem in electronics has been that the penalty due to the performance degradation of interconnects with the technology scaling. Scaling defines the reduction of the dimensions of transistor and interconnects. Scaling increases the number of devices per unit area with more functionality in same area and increasing the performance of the transistor but decreasing the performance of interconnect especially in global interconnect level. Hence delay will be increased in global interconnects. Copper (Cu) interconnects has limitations such as electro migration, electron scattering when it is scaled below 32nm technology. We propose the material and signalling solution to the on chip interconnect design problems. CNT interconnects can be used to overcome these limitations imposed by scaling. In this paper important aspects associated with the modeling and simulation of global multiwalled CNT (MWCNT) is analyzed. The MWCNT Characterized by Multi Conductor Circuit Model (MCC) & Equivalent Single Conductor Model (ESC). Based on ESC Model, an efficient Techniques Combining Decoupling Model & Delay Extraction is presented for Fast Simulation of MWCNT interconnects. Performances metrics of this interconnect are delay, power and bandwidth. These carbon nanotube based interconnects are simulated using HSPICE software.

KEY WORDS: Carbon nanotube (CNT), circuit model, interconnect, multi-walled CNT (MWCNT), performance analysis, signal delay, single-walled CNT (SWCNT).

1. INTRODUCTION

In High speed IC design, interconnects play a major role in determining the circuit performance. The continuous performance degradation of on-chip Cu/low-k interconnects is one of the greatest challenges to keep Moore's law alive while the scaling of transistors. The device and the dimensions have been shrunk according to scaling.

As wire width decreases, the resistance of traditional copper interconnects rapidly increases under the combined effects of grain boundary scattering and surface scattering which will lead to vulnerable delay and electro migration problem in nanometer region. These issues limit the interconnect performance and reliability of VLSI systems.

So, several researches have been undergone by various research groups to find the alternate interconnect material for copper to alleviate these limitations. According International Technology Roadmap for Semiconductors (ITRS), the alternative interconnect materials are Carbon Nano Tube (CNT), Graphine Nano Ribbon (GNR), Si-Nanowires. Optical interconnect and wireless interconnect.

Among the alternate materials, CNT has chosen as interconnect material for future generation IC's due to its extraordinary electrical properties, high thermal conductivity, high current carrying capability and mechanical stability. CNTs have long mean free path (MFPs) in the order of several micrometer (40nm for cu), which provides low resistivity and ballistic transport.

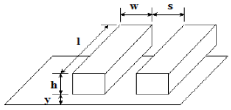
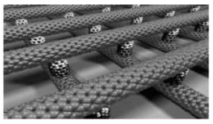


Figure.1.(a) Interconnect geometry



(b) Structure of CNT

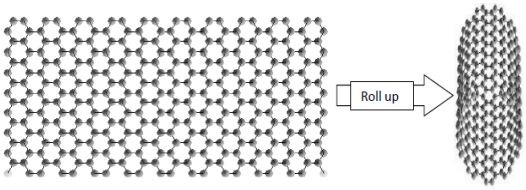


Figure.2. Carbon nanotube structure

The graphene sheet can be rolled in many possible ways. Depending on which direction CNT are rolled up (chirality), they demonstrate either metallic or semiconducting properties.

- Armchair, $\alpha = 30^o$, exhibits metallic behavior.
- Zig-zag, $\alpha = 0^o$, exhibits semiconducting behavior.
- Intermediate, $\alpha = 0^o < \alpha < 30^o$

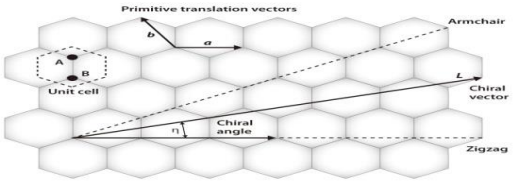
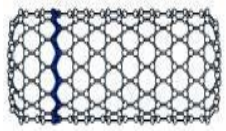


Figure.3. Illustration of chiral vector C in terms of vector a1 and a2

The structure of armchair and zigzag of CNT is shown in Fig 4.



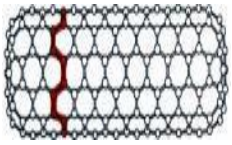


Figure.4. (a) Zigzag **(b) Armchair**

In this project, modeling of MWCNT at various interconnects levels (local, semi global and global) in 22 nm and 16 nm technologies have been done. The MWCNT interconnects are analyzed by using ESC in Hspice simulator. The performance parameters will be delay, power delay product and band width are obtained and compared against Cu.

On-Chip Interconnects & it's Equivalent Circuit Model:

Aluminium Interconnects: For several semiconductor technology generations, aluminium was used as the on-chip interconnects metal and silicon-di-oxide as the inter- and intra-level insulator. With rapid scaling of feature size to deep submicron levels, the signal delay caused by interconnect became increasingly significant compared to the delay caused by the gate and thus affecting the circuit's reliability. Copper has a higher melting point (1,357 K) than aluminium (933K), which gives copper the advantage over aluminium in electro migration and stress migration.

Copper Interconnects: The shrinkage in the feature size of Cu interconnects limit the interconnect performance and reliability in terms of delay, power and bandwidth. To analyse these parameter by using HSPICE simulator. Figure.5, Shows the equivalent RLC model for copper interconnect.

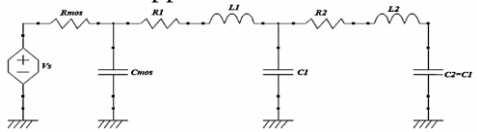


Figure.5. Equivalent RLC circuit model for copper interconnect

Using this model, interconnect resistance *R*, capacitance *C* and inductance *L* were calculated for various length.

$$R = \frac{\rho\, l}{wt} \quad (1)$$

$$C = \varepsilon\left[\frac{w}{h} + \left\{2.22\left(\frac{s}{s+0.7h}\right)^{3.19}\right\} + 1.17\left(\frac{s}{s+1.51h}\right)^{0.76}\left(\frac{t}{t+4.53h}\right)^{0.12}\right\} \quad (2)$$

$$L = \mu l/2\pi[ln(\frac{2l}{w+t} + \frac{1}{2} + \frac{0.22(w+t)}{l}] \quad (3)$$

$$M = \mu\frac{l}{2\pi\left[ln\left(\frac{2l}{d}\right) - 1 + \frac{d}{l}\right]} \quad (4)$$

Where R-Resistance, ρ-Resistivity, *l*-Length of interconnect, *w*-Width, *s*-Spacing, *t*-Thickness, *d*-distance between two layers, ε_O-Dielectric permittivity, ε_r-Relative dielectric permittivity of copper, μ -Permeability.

In this paper, we have assumed that the spacing between interconnects *s* is equal to the interconnect width, i.e. *s* = w. Also the distance between two layers of interconnects *d* is assumed to be equal to twice as that of the interconnect width, i.e. *d* =2w. Furthermore, the thickness of the interconnect *(*t=AR*W) can be changed according to the aspect ratio (AR).

CNT Interconnects: CNT was discovered by Iijima in 1991. CNTs are sheet of graphene rolled up as hollow cyllinder. These tubes have a diameter of the order of nm, hence the name. They can be classified as Single-Walled CNT (SWCNTs), Multi-Walled CNT (MWCNTs), Double-Walled CNT (DWCNTs).

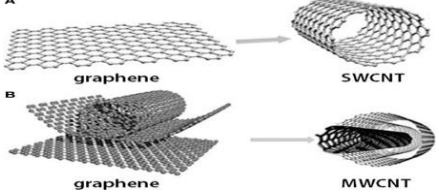


Figure.6. CNT as various structure

A single graphene sheet is rolled up to form SWCNT with diameter vary from 0.4 to 4nm. DWCNT and MWCNT are the two and multiple concentric shells of graphene sheets rolled up together. This reduces the resistance and rise the Mean free path (MFP).

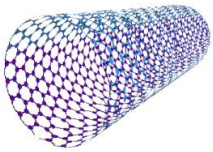
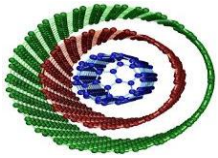


Figure.7. (a) SWCNT



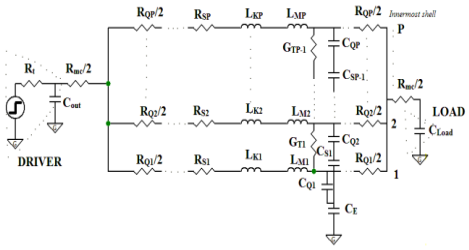
(b) MWCNT

SWCNT Interconnects: As the feature size of Cu interconnects shrinks, which has performance degradation in interconnects. SWCNT has been proposed for the realization of future interconnects. SWCNT consists of a single sheet of graphene rolled up as hollow cylinder.

MWCNT Interconnects: MWCNT consists of several concentric graphene cylinders, whose outer diameter may vary from a few to 100nm, the spacing between the walls is 0.32 nm, the same as the spacing between graphene sheets in graphite. Each cylinder in MWCNT has different diameter. It has been confirmed both theoretically and experimentally that all shells within MWCNT can conduct if proper connections are made to all of them. High quality MWCNT has very large mean free path and operates in gigahertz frequency range. The theoretical models propose that long MWCNT with large-diameter can outperform Cu and even SWCNT interconnects. Hence it will be suitable for all level of interconnects.

Out of these CNTs, MWCNT are proven as the most powerful one due to its ease of fabrication and have lower resitivity than SWCNT-bundles. MWCNT shows better metallic behavior. It provides significant performance improvement compared to Cu. Hence, MWCNTs has been considered as global interconnect for future IC design.

The equivalent circuit model of MWCNT is shown in below MWCNTs are modeled as Multi-Conductor-Transmission Line model (MCC), but it would be complicated and consume more time to simulate. To mitigate this problem, a simplified ESC.



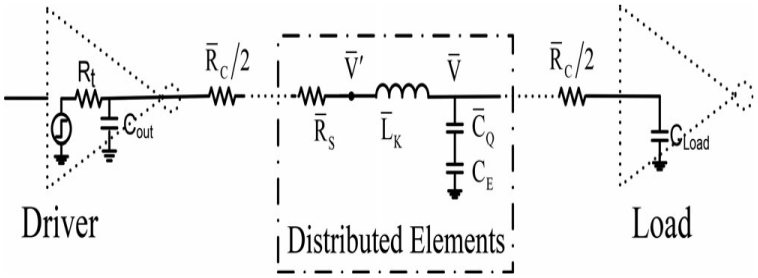


Figure.8. (a) Equivalent MCC model of MWCNT

(b) Equivalent ECC model of MWCNT

The no of channels can be calculated from the formula.

$$N = a.D + b, \quad D>3nm \tag{6}$$

Where a=0.0612 nm^{-1} b=0.425 D-diameter of the shell

MFP(λ)=1000D, D-diameter of the shell:

$$D_i = D_{max} - 2d\,(i-1) \tag{7}$$

The no of channel channels of i^{th} shell is given by

$$N = a.Di + b \tag{8}$$

Using this model, interconnect resistance *R*, capacitance *C* and inductance *L* were calculated

$$R = R_Q + R_S.L = \frac{h}{2Ne^2} + \frac{h}{2Ne^2}\left(\frac{L}{\lambda}\right) \tag{9}$$

$$L_{magnetic} = \left(\frac{\mu}{2\pi}\right)\cosh^{-1}\left(\frac{2H}{D}\right) \tag{10}$$

$$L_{K/Channel} = \left(\frac{h}{2v_f}\right)\left(\frac{1}{2}\right) = 8\ nH/\mu m \tag{11}$$

$$L_{K/Shell} = L_{\frac{K}{Channel}}/(a.D + b) \tag{12}$$

$$C_{Q/Channel} = 2\left(\frac{2e^2}{hv_f}\right) = 193\ aF/\mu m \tag{13}$$

$$C_{Q/Shell} = C_{Q/Channel} * (a.D + b) \tag{14}$$

$$C_S = \frac{2\pi\epsilon}{\ln\left(\frac{D_{out}}{D_{in}}\right)} = \frac{2\pi\epsilon}{\ln\left[\frac{D_{out}}{D_{out}-2d}\right]} \tag{15}$$

Where R_Q-Quantum contact resistance, R_S- scattering induced resistance, L-length of the shell, λ-mean free path (MFP), N-no of conducting channels, $L_{magnetic}$-magnetic inductance, L_K-kinetic inductance H-separation between the nanotube center and ground, D-diameter of each shell, C_Q-quantum capacitance, C_S-shell to shell capacitance, C_E-electrostatic capacitance, G_T-tunneling conductivity, M-mutual inductance.

Performance Analysis of Copper and Cnt Interconnects: The CNT and Cu interconnects are studied through simulations in 22nm & 16nm technology using Synopsys HSPICE. The Avanwaves tool is used as a waveform viewer. Interconnect is modeled as distributed RLC model. The various performance matrices like delay, power and bandwidth of MWCNT & Cu are obtained from simulation results for different technologies are given in the following sections.

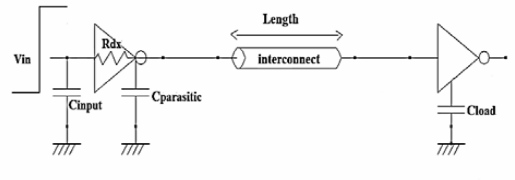


Figure.9. Performance test circuit.

The following simulation results are copper and MWCNT at 22nm along with different interconnect levels.

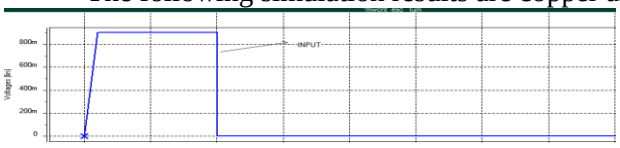
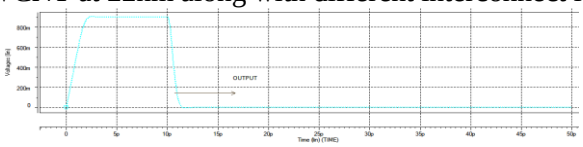
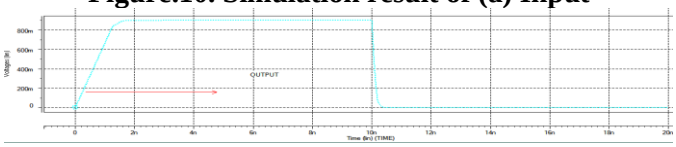


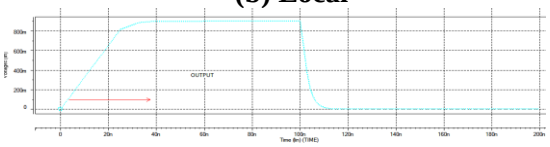
Figure.10. Simulation result of (a) Input



(b) Local



(c) Semi global



(d) global

The local interconnects are the shortest interconnects used to connect adjacent gates or devices. The length of the interconnect is in the range of few hundred nanometers to few micrometers. It has high resistance because of the small area of cross section. MWCNT has better performance than copper because it uses CNT with smaller diameter and hence it achieves ballistic transport.

The intermediate interconnects are also called semi global interconnects and used to make connection between the logic blocks inside the IC. Its length ranges from tens of micrometer to five hundred micrometer. Global interconnects are the longest interconnects that run across the chip. It ranges in the order of millimeters. It has larger cross sectional area.

Delay: Figure 10 shows the comparison of delay in MWCNT and Cu in various technology nodes (22 nm and 16nm). The scale of the delay axis is taken in logarithmic measurement. With the increase in the length of the interconnect carbon nano structures outperform the Copper interconnects. Deep analysis of the results obtained in 22nm technology node, explains that, MWCNT have minimal delay compared to Cu In Local interconnect MWCNT are having nearly three orders less delay than Copper , due to its ballistic transport and excellent thermal and electrical conductivity,

The measurement of delay for all the three interconnects at different level is shown in table 1.

Table 1. Delay comparison of Cu and MWCNT interconnect at 22nm in PSEC

LENGTH OF INTERCONNECTS	MWCNT	Cu
1u	0.341	248000
3u	1.25	248000
100u	39	272000
200u	133	292000
500u	400	385000
1000u	1400	375000

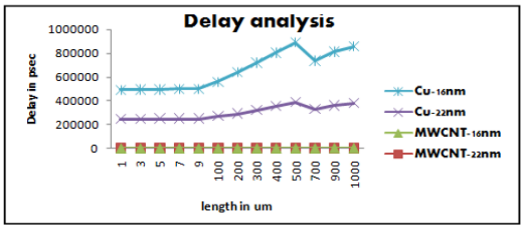


Figure.11. Delay comparison between Cu and MWCNT in 22nm and 16nm technology nodes.

Power Delay Product (PDP): Table.2, shows that PDP comparison of MWCNT and Copper. It has been observed that carbon nano structures have very less power delay product almost 3 order lesser than copper due to its excellent

thermal conductivity and large conductance to the electric current flow. Figure.11, shows the PDP Comparison of MWCNT and Cu. Simulation results shows that MWCNT has lower PDP when compared to Copper by 1000 times.

Table.2. Comparison of PDP at 22nm

Interconnect level	MWCNT	Cu
Local	2.21 aJ	98.8 fJ
Semi-global	216.9 aJ	174 fJ
Global	2223 aJ	240 fJ

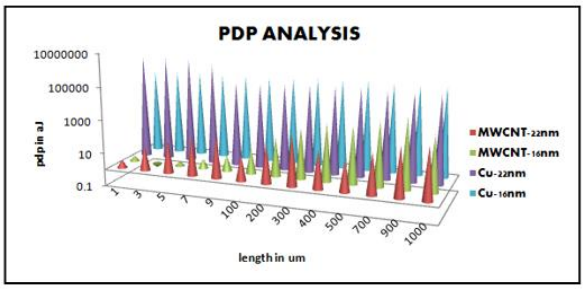


Figure.12. Comparison of power delay product of MWCNT and Copper

Band width: Bandwidth comparison of copper and MWCNT for 22nm and 16nm technology nodes is shown in Table.3. Bandwidth is calculated by 0.35/rise time**.** MWCNT have wide bandwidth compare to copper interconnect in the range of terahertz, thus MWCNT is more suitable candidate for high speed operation for future interconnects technology than copper.

Table.3. Comparison of Band width at various nodes

Technology nodes		Interconnect level (in µm)		
		Local	Semi- global	Global
22nm	Copper	460KHz	410KHz	307KHz
	MWCNT	0.229THz	324MHz	15MHz
16nm	Copper	455KHz	376KHz	246KHz
	MWCNT	0.223THz	325MHz	118MHz

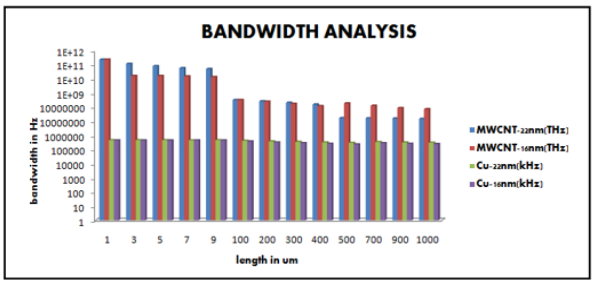


Figure.13. Comparison of bandwidth of MWCNT and Copper

2. CONCLUSION

In this paper, we have compared the performance of on-chip interconnects Cu and CNT. Simulation results show that MWCNT has low delay and high speed compared to Cu in local, semi global and global interconnects. It is clearly shown that MWCNT is 10 order (THz) times better than Cu in terms of bandwidth. In 22nm & 16nm technologies, simulation results show that CNT interconnect shows better performance in delay, bandwidth and PDP than copper interconnects. It has been observed that CNT performing better when technology scales from 22nm to 16nm but copper has performance degradation. From the above analysis, it has been concluded that the, MWCNT can be used as on–chip interconnect and also it obeys the moore's law for future technology nodes. Among all types of CNT (SWCNT, SWCNT Bundle) interconnects, MWCNT shows significant improvement in delay, PDP and bandwidth than Cu. Hence, in future technology node MWCNT will obey the moore's law.

In future, Current mode signaling will be used in MWCNT interconnect to provide better performance than all other interconnecting materials. We can Analyze the impact of crosstalk when current mode signaling through CNT interconnect using HSPICE simulator.

REFERENCES

Amore M.D, Sarto M.S and Tamburrano, Fast transient analysis of next-generation interconnects based on carbon nanotubes, IEEE Trans Electromagn Compat, 52 (2), 2010, 496–503.

Ferranti F, Antonini G, Dhaene T, Knockaert L and Orlandi A, Compact and accurate models of large single-wall carbon-nanotube interconnects, IEEE Trans Electromagn Compat, 53 (4), 2011, 1025–1033.

Hong Li, Wen-Yan Yin, Kaustav Banerjee, and Jun-Fa Mao, Circuit Modeling and Performance Analysis of Multi-Walled Carbon Nanotube Interconnects, IEEE Transactions on Electron Devices, 55 (6), 2008.

Li H, Xu C, Srivastava N and Banerjee K, Carbon nanomaterials for next-generation interconnects and passives, Physics, status, and prospects, IEEE Trans Electron Devices, 56 (9), 2009, 1799–1821.

Lu J.Q, Tang M and Mao J.F, Fast crosstalk analysis of multi-walled carbon nanotube interconnects, in Proc Electr Des Adv Packag Syst. Symp, 2012, 131–134.

Naeemi A and Meindl J.D, Compact physical models for multiwall carbon-nanotube interconnects, IEEE Electron Device Lett, 27 (5), 2006, 338–340.

Naeemi A and Meindl J.D, Compact physics-based circuit models for graphene nanoribbon interconnects, IEEE Trans Electron Devices, 56 (9), 2009, 1822–1833.

Nieuwoudt A and Massoud Y, on the optimal design, performance and reliability of future carbon nanotube-based interconnect solutions, IEEE Trans Electron Devices, 55 (8), 2008, 2097–2100.

Nishad A.K and Sharma R, Analytical time domain models for performance optimization of multilayer GNR interconnects, IEEE J Sel Topics Quantum Electron, 20 (1), 2014, 1699–1705.

Pu S.N, Yin W.Y, Mao J.F and Liu Q.H, Crosstalk prediction of single- and double-walled carbon-nanotube (SWCNT/DWCNT) bundle interconnects, IEEE Trans. Electron Devices, 56 (4), 2009, 560–568.

Srivastava N, Li H, Kreupl F and Banerjee K, On the applicability of single-walled carbon nanotubes as VLSI interconnects, IEEE Trans Nanotechnol, 8 (4), 2009, 542–559.